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**CORRESPONDENCE COURSE**

**MASTER OF SCIENCE IN ASIC DESIGN (PREVIOUS) DEGREE EXAMINATIONS  
FEBRUARY-2009**

Time: 3 hours

Max marks: 80

**ADEC11: Basic VLSI and Analog VLSI Design**

Note: Answer any four full questions. All questions carry equal marks.

1. a) Explain the basic MOS enhancement mode and depletion mode transistor characteristics and its actions. (10)  
b) With a neat diagrams, explain the n-well fabrication process. (10)
2. a) Discuss the following electrical properties of MOS transistor. (10)  
i) Drain to Source current versus Voltage relationships. ii) Transconductance. (10)  
b) With relevant circuits explain pass transistor AND gate and nMOS inverter. (10)
3. a) Derive an expression for pull-up to pull-down ratio for an n-MOS inverter driven by another nMOS inverter. (10)  
b) Explain the sheet resistance concept applied to MOS transistors and inverters. (10)
4. a) Show how delay unit and Inverter delays are achieved? (10)  
b) Explain design process of Switch logic implementation of four-way Multiplexer circuit. (10)
5. a) What is D- Latch? Explain design rules and layouts for the D-Latch. (10)  
b) Explain the features of pseudo nMOS and Tristate circuits. (10)
6. Write notes on the following (10 X 2)  
a) Stick diagram design rules. b) Code converters

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**ADEC 12: ASIC Design**

Time: 3 Hours

Max Marks: 80

Note: Answer ANY Four Questions. All questions carry equal marks

Q. 1

- (a) Give one example of data path logic cell with proper diagram. (10)  
(b) Explain the difference types of MGA or Gate array ASICs. (10)

Q. 2

- (a) Show with illustration logic minimization using PLA tools. (10)  
(b) Write the EDIF description for the half gate ASIC. (10)

Q.3

- (a) Explain the following technologies for programmable ASICs. (10)  
i) Anti-fuse ii) EEPROM  
(b) Give the design of the 4T SRAM cell and explain the READ and WRITE operation. (10)

Q.4

- (a) Explain with proper diagram the microcell of Xilinx CPLD. (10)  
(b) With the proper block diagram explain XC9500 CPLD Architecture? (10)

Q. 5

- (a) What are PLD's ? Discuss different PLDs. (10)  
(b) Calculate power dissipation and clock spine interconnect for the following specification 35,000FFs, input capacitance of clock input to each FF is .015pf. Clock frequency is 250 MHz,  $V_{dd} = 3.3$  V, Chip size is 20mm on a side, clock spine consists of 200 lines across the chip, interconnect capacitance is 2pf/cm. (10)

Q. 6 Write short notes on any four of the following. (5 X 4)

- a) Library architecture  
b) AC input I/O cell  
c) Power dissipation in ASIC  
d) emlore's constant  
e) Types of ASIC.

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**ADEC 13: CAD tools for VLSI**

Time: 3 Hours

Max Marks 80

Note: Answer ANY Four Questions. All questions carry equal marks

Q.1

- (a) Write and explain a Kruskal's and Prim pseudo code algorithm for minimum spanning tree.(10)  
 (b) Find the shortest path from 'A' to all vertices for below graph? (10)



Q.2

- (a) Write the pseudo code for ASAP algorithm and ALAP algorithm and explain briefly.(10)  
 (b) Define mobility. With an example determine mobility of each functional unit using ASAP and ALAP algorithm. (10)

Q.3

- (a) Describe the System level, Board level and chip level partitioning with their objectives.(10)  
 (b) Explain the partitioning problem formulation and respective parameters for to be considered. (10)

Q.4

- (a) What is a main goal of pin assignment? Write pseudo code for linear channel pin assignment the uses L,J,K solutions. (10)  
 (b) With pseudo code explain simulated annealing algorithm for placement. (10)

Q.5

- (a) Write pseudo code for simulated evolution algorithm used in floorplanning. (10)  
 (b) Classify partitioning algorithm based on initial partitioning, nature of algorithm and nature of process used for partitioning. (10)

Q.6 Answer any four of following

(5 X 4)

- (a) Scheduling pipelined circuits. (b) Rectangular Dualization  
 (c) Maze routing algorithm (d) MMM algorithm  
 (e) H-tree based algorithm

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**CORRESPONDENCE COURSE**

**MASTER OF SCIENCE IN ASIC DESIGN (PREVIOUS) DEGREE EXAMINATIONS  
FEBRUARY-2009**

**ADEC111 - Digital circuit design using VERILOG**

Duration: 3 hrs.

Max Marks: 80

**Note: Answer any four full questions  
All questions carry equal marks**

- 1 a) Write three different descriptions of a 2-bit full adder including carry-in and carry-out ports. One description should use gate-level models, another should use continuous assignment statements, and the third — combinational of both.  
b) What are the differences between *if-else* and the ("?:") conditional operator?
- 2 a) Write a verilog code for 4-bit comparator.  
b) Write a verilog code for 8:1 multiplexer using two 4:1 multiplexer and one 2:1 multiplexer.
- 3 a) Write the Verilog RTL description for a 4-bit binary counter with synchronous reset that is active high. Write a test bench for testing the code.  
b) How to choose between a *case* statement and a multi-way *if-else* statement?
- 4 a) Draw the circuit diagram for an Xor gate, using nmos and pmos switches. Write the Verilog description for the circuit.  
b) Can the *generate* construct be nested? Illustrate the side effect of not connecting all the ports during Instantiation
- 5 a) Design a 3-to-8 decoder, using a Verilog RTL description. A 3-bit input a[2:0] is provided to the decoder. The output of the decoder is out[7:0]. The output bit indexed by a[2:0] gets the value 1, the other bits are 0.  
b) Define a positive edge-triggered D-flipflop with clear as a UDP. Signal clear is active low.
- 6 Using a synchronous finite state machine approach, design a circuit that takes a single bit stream as an input at the pin in. An output pin match is asserted high each time a pattern 10101 is detected. A reset pin initializes the circuit synchronously. Input pin clk is used to clock the circuit.

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**ADEC 1)2: RF Microelectronic Chip Design**

Time: 3 Hours

Max Marks: 80

Note: Answer ANY Four Questions. All questions carry equal marks.

- 1 a) What are the applications of RF technology. (5)  
b) Explain the effects of non linearity with the respective mathematical equations.(15)
- 2 a) Distinguish between coherent and non-coherent detection with diagrams. (6)  
b) Distinguish between FDMA and TDMA. List the advantages and disadvantages of them over one another. (14)
- 3 a) Describe the behavior of a BJT at RF frequencies. (4)  
b) With a diagram arrive at a CMOS LNA from common source stage. (8)  
c) Write a note on CMOS mixers. (8)
- 4 a) Explain a VCO with diagram. Obtain its mathematical model and show that a VCO has a tendency to reject high frequency components at its input. (10)  
b) What is phase noise? What are the effects of phase noise in RF communication? (10)
- 5 a) Describe noise power trade off. (4)  
b) Write a note on Tuning issues in oscillators. (8)  
c) Explain a resonatorless VCO. (8)
- 6 a) Explain a basic PLL with it's waveforms. Describe its response to a small frequency step. (10)  
b) Explain what are charge pump PLL's. (6)  
c) Write a note on noise in PLL. (4)

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**ADEC 121: PLD AND FPGA**

Time: 3 Hours

Max Marks: 80

Note: Answer ANY Four Questions. All questions carry equal marks.

- 1 a) What are PLA's. Explain with a diagram 4\*3 PLA. Write the logic functions for their outputs. (8)
- b) What are PAL devices. Explain the logic diagram of PAL 168. (8)
- c) What are the advantages of PAL over PLA. (4)
- 2 a) What are FPGA's. Explain Xilinx 3000 series FPGA. (10)
- b) Explain an interconnect schemes with diagram in Altera FLEX. (6)
- c) Distinguish between CPLD and FPGA's. (4)
- 3 a) With diagrams explain and distinguish between Mealy and Moore machines. (10)
- b) What is metastability. How is it achieved in PLD's. (6)
- c) Explain what is Synchronization. (4)
- 4 a) Explain the terms Clock trees, Clock skew and Pipelining in digital design. (6)
- b) With a diagram explain a Mealy Machine. (8)
- c) Explain how synchronization can be achieved in digital design. (6)
- 5 a) What is entity declaration? Explain an example of entity declaration. (6)
- b) Explain and distinguish between concurrent and sequential signal assignment. (8)
- c) What is delta delay? Explain delta delays in concurrent signal assignment statements. (6)
- 6 a) What is package declaration? Give its syntax. (6)
- b) What are implicit and explicit visibility. (4)
- c) Explain the terms library clause and use clause with their syntax. (8)

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Duration: 3 hrs.

**ADEC122 - Low Power VLSI Design**

Max Marks: 80

**Note: Answer any four full questions  
Each question carries 20 Marks**

1. a. Briefly outline the needs for low power VLSI chips and explain the various sources of power dissipation.  
b. The chip size of a CPU is 15mm X 25mm with clock frequency of 300 MHz operating at 3.3V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock signal is routed on a metal layer with width of 1.2 $\mu$ m and the parasitic capacitance of the metal layer is 1fF/ $\mu$ m<sup>2</sup>. What is the power dissipation of the clock signal? 10 + 10
2. a. Discuss the following with respect to low power design
  - i. Self gating flip flop
  - ii. Double edge triggered flip flop
 b. With circuit examples explain the different transformation methods used for gate reorganization. 10 + 10
3. a. Explain the Bus invert encoding with relevant expressions.  
b. Explain the guarded evaluation technique to reduce switching activities.  
c. Explain Logic encoding for low power consumption with an example. 6 + 6 + 8
4. a. Discuss about Dual bit type signal model and derive the power model of a simple single input and single output FIFO under the uniform white noise region.  
b. Derive the expression for Dynamic power dissipation. 10 + 10
5. a. Discuss about low swing bus circuit techniques.  
b. Explain the loop unrolling transformation with an example. 10 + 10
6. a. What is Boolean decision diagram? How it helps itself in implementing pass transistor logic?  
b. How does the complementary adiabatic logic computation differ from the static CMOS gate in power dissipation? 10 + 10