



MANGALORE UNIVERSITY

DIRECTORATE OF CORRESPONDENCE COURSES,

MANGALAGANGOTTHRI - 574 199

PROSPECTUS

POST GRADUATE PROGRAM

MASTER OF SCIENCE IN

ASIC DESIGN

STUDY CENTER

**Rastreyra Sikshna Samithi Trust
R.V.Center For Cognitive Technologies,
R.V. Teachers College Building, 2nd Block, Jayanagar,
Bangalore – 560 011.India
Phone: +91-80-26578577 / 67178105**

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MANGALORE UNIVERSITY

CORRESPONDENCE EDUCATION PROGRAMS

Objectives

Mangalore University has launched correspondence education programs as per the National Education Policy in order to reach higher education to all sections of the society. The objectives of these programs are:

- a) Promote higher education through non-formal means, specifically through correspondence mode.
- b) Promote the concept of correct intelligence among students and teachers.
- c) Establish networking of learners and knowledge practitioners by means of Information and Communication Technology
- d) Offer both conventional and innovative courses for knowledge proliferation.
- e) Take such courses to the doors of socially and economically disadvantaged sections of the society.
- f) Collaborate with national and international educational organizations to promote excellence in non-formal education.
- g) Export quality higher education through communication networks.
- h) Encourage disadvantaged and weaker sections to acquire essential skills, information and knowledge to cope with the demands of emerging new professions in a fast changing global society.
- i) Perform such other functions as and when specified/prescribed by university.

**REGULATIONS GOVERNING THE POST-GRADUATE DEGREE PROGRAMS
THROUGH CORRESPONDENCE COURSE**

(Framed under section 44(1) read with para 4(i) of the KSU act 2000)

1. TITLE AND COMMENCENT:

- i) These regulations shall be called “the regulations governing the post graduate degree programs through correspondence course of **Mangalore University**
- ii) These regulations shall come into effect from the date of assent of the Chancellor.

2. PROGRAMS:

The following post graduate degree programs shall be introduced through correspondence course.

- A) *Master of Science in ASIC Design.***
- B) *Master of Science in Mobile Communication & Internet***
- C) *Master of Science in Information Technology***

Any other post graduate degree programs in the faculties of Science, Technology and Management introduced from time to time under correspondence course shall become part of this regulation.

3. ELIGIBILITY:

(a) Master of Science in Application Specific Integrated Circuit (ASIC) Design

&

(b) Master of Science in Mobile Communication and Internet Technologies

Candidates who have passed bachelors degree in Engineering / AMIE/ AMIETE (Electrical / Computer Science Streams) / Equivalent

OR

Bachelor of Science Degree with the following Optional subjects: Electronics / Physics / Computer Science / Information Technology / Computer Applications or Bachelor of Computer applications of Mangalore University or any other University considered as equivalent thereto by Mangalore University with one year Industrial Experience in relevant area.

(c) Master of Science in Information Technology

Candidates who have passed Bachelors degree in Engineering / AMIE / AMIETE (Electrical / Computer Science Streams) / Equivalent

OR

Bachelor of Science Degree with the following Optional subjects: Electronics / Physics / Computer Science / Information Technology / Computer Applications or Bachelor of Computer Applications of Mangalore University or any other University considered as equivalent thereto by Mangalore University with one year Industrial Experience in relevant area.

OR

Bachelors degree of any recognized University with one year PGDCA / PGDIT from any recognized University or DOEACC`A' Certificate or GNIIT or DAC from C-DAC / MOSE / PGDST from CIST or PGDEDPCM from Bharatiya Vidya Bhavan or Graduation + 3 years Professional IT Experience / IT Teaching Experience. Candidates with Master degree in Geo Informatics/ Bio Informatics are also eligible.

4. DURATION:

The Post graduate degree programs shall be of 2 academic years

5. MEDIUM OF INSTRUCTION:

The Medium of Instruction and examination shall be English

6. MAXIMUM PERIOD FOR COMPLETION OF THE MASTERS PROGRAM

The candidate shall complete the masters degree programs within the period as prescribed in the regulations governing maximum period for completing various degree or diploma programs offered by Mangalore University under regular scheme. No candidate shall be permitted to appear the examination after prescribed period for completing the program

A candidate who fails in any subject (1st – 2nd) year may be permitted to take the examinations again at a subsequent appearance as per the syllabus and scheme of examination in vogue at the time the candidate took the examination for the first time. This facility shall be limited to the following four years.

7. CONTACT PROGRAM

There shall be 2 contact programs of 15 days duration each in a year. Seminars, discussions and lab-sessions will be part and parcel of the contact programs.

8. SCHEME OF EXAMINATION for Master of Science in ASIC DESIGN

PREVIOUS

PAPER	NAME OF THE SUBJECT	DURATION OF EXAM IN HOURS	MARKS FOR		
			INTERNAL ASSESSMENT	EXAM	TOTAL
PAPER 1	BASIC VLSI & ANALOG DESIGN	3	20	80	100
PAPER 2	ASIC DESIGN	3	20	80	100
PAPER 3	CAD TOOL FOR VLSI	3	20	80	100
PAPER 4	ELECTIVE I	3	20	80	100
PAPER 5	ELECTIVE II	3	20	80	100
Total:		15	100	400	500

Elective – I	Elective - II
1.DIGITAL CIRCUIT DESIGN USING VERILOG	1. PLD AND FPGA
2. RF MICRO ELECTRONIC CHIP DESIGN	2. LOW POWER VLSI DESIGN

FINAL

PAPER	NAME OF THE SUBJECT	DURATION OF EXAM IN HOURS	MARKS FOR IA	EXAM	TOTAL
PAPER- 6	VLSI TECHNOLOGY & SYSTEM ON CHIP	3	20	80	100
PAPER- 7	ELECTIVE III	3	20	80	100
PAPER- 8	PROJECT WORK THESIS EVAL. & VIVA VOCE	-	100	300 100	500
TOTAL:		6	140	560	700

Elective III
1. VLSI AND DSP-DRIVEN COMPUTER SYSTEMS
2. NANOELECTRONICS

9. INTERNAL ASSESSMENT

Marks for internal assessment shall be awarded on the basis of assignments. Students shall submit two assignments of 10 marks each in paper of study which shall be evaluated by the faculty concerned. The assignment marks should be forwarded to the registrar (Evaluation) at least 15 days before the commencement of annual examinations.

10. REGISTRATION FOR EXAMINATION

A candidate shall register for all the papers of the current year, when he/she appears for the examination for the first time.

11. CARRY OVER PROVISION:

Candidates who fail in the first year can go to final year and take the examinations at the end of the second year.

12. MINIMUM FOR PASS

No candidate shall be declared to have passed in a examination unless he/she obtains not less than 35% marks in each paper and 40% marks in the aggregate of theory and internal marks put together.

13. CLASSIFICATION OF SUCCESSFUL CANDIDATES:

- i) The results of successful candidates at the end of the final year shall be classified on the basis of aggregate marks obtained in the previous and the final year.
- ii) The candidates who pass all the examinations in the first attempt are eligible for rank provided they secure 60% and above marks.
- iii) The results of the candidates who have passed the final year but not passed previous year examinations shall be declared as NCL (not completed lower examinations).such candidates shall be eligible for the degree only after completion of the previous year examinations.

Percentage of marks for declaring class:

Distinction	70% and above
First Class	60% and above but less than 70%
High Second Class	55% and above but less than 60%
Second Class	50% and above but less than 55%
Pass Class	40% and above but less than 50%

14. REJECTION OF RESULTS:

- i. A candidate who fails in one or more papers of a year (previous / final) may be permitted to reject the result of the whole examination of that year. Rejection of result paper-wise shall not be permitted. A candidate who rejects the results shall appear for the examination of that year in the subsequent examination.
- ii. Rejection shall be exercised only once in each examination and the rejection once exercised cannot be revoked.
- iii. Application for rejection along with payment of the prescribed fee shall be submitted to the Director of Distance Education together with the original statement of marks within 30 days from the date of publication of the result.
- iv. A candidate who rejects the result is eligible for only class and not for ranking.

15. IMPROVEMENT OF RESULTS

- i. A candidate who has passed in all the papers of a year (previous / final) maybe permitted to improve the result by reappearing for the whole examination of that year.
- ii. The reappearance shall be permitted only once in each year (previous / final).
- iii. The reappearance for the examination of any year is permitted during the subsequent examination of that year.
- iv. Application for improvement along with payment of the prescribed fee shall be submitted to the Director of Correspondence Education together with the original statement of marks within 30 days from the date of publication of the result.
- v. If the candidate passes in all the subjects in the reappearance, higher of the two aggregate marks secured by the candidate shall be awarded to the candidate for

that year (previous / final). In case the candidate fails in the reappearance, candidate shall retain the first appearance result.

- vi. A candidate who has appeared for improvement is eligible for only class and not for ranking.

16. INTERNAL ASSESSMENT MARKS

Internal assessment marks shall be shown separately in the marks card. A candidate who has rejected the result or who, having failed, takes the examination again or who has appeared for improvement shall retain the internal assessment marks already obtained.

17. Fee Structure

Tuition Fee	40,000.00
Laboratory Fee	8,000.00
Library Fee	2,000.00
Total	50,000.00

Per Annum

18. Conditions governing the program

1. Candidate admitted to a degree course in the university shall not be permitted to study simultaneously any other program leading to a degree in this or any other university.
2. If a candidate gets admitted to more than one post graduate or degree course, the Director of Correspondence Courses shall cancel his/her admission to both the courses
3. Candidates shall abide by the Rules and Regulations in force and those to be issued by the Mangalore University from time to time.

4. False declaration of age, qualification etc. by the candidate will disqualify his/her admission to the course.
5. This prospectus provides all necessary information to the candidates. Hence candidates are advised to keep the prospectus till the completion of the program. Unnecessary correspondence about the details already available in this prospectus shall be avoided.
6. Provisional pass certificate will be issued by the Registrar (Evaluation), Mangalore University on request and on payment of prescribed fee, after the declaration of the result by the university.
7. After the admission is approved by the university, Identity cards will be issued. If original card is lost, duplicate card may be obtained from the office of the Director, RVCCT, on payment of Rs.500/- through bank challan at ING-Vysya Bank or through DD drawn in favor of R.V. Centre For Cognitive Technologies.
8. Any change of address should be intimated to the Director of Correspondence Courses or Director, RVCCT. However it may be noted that any change of address in the middle of the academic year will cause unavoidable delay.
9. The study materials, circulars, letters, examination notifications and such other correspondences shall be sent by ordinary post only. The same may be collected in person from Office of the Director, R.V. Centre For Cognitive Technologies, R.V. Teachers College Building, 2nd Block, Jayanagar, Bangalore – 560 011.

**SYLLABUS FOR
MS - ASIC DESIGN**

PREVIOUS

PAPER 1

BASIC VLSI AND ANALOG VLSI DESIGN (ADEC11)

1. Introduction to MOS technology:

Introduction to IC technology, Basic MOS Transistor Enhancement Mode, Depletion Mode, Threshold Voltage, Body Effect, VLSI Design flow, VLSI Design Styles.

2. Fabrication Process:

NMOS, CMOS, P Well, N Well process, Twin Tub Process, Silicon on insulator

3. Electrical Properties of MOS Circuits :

Drain to Source Current VS Voltage relationship, MOS Transistor, transconductance and output conductance, figure of merit, pass transistors, NMOS inverters, determination pull up to pull down ratio for NMOS inverter driven by another NMOS inverter, determination pull up to pull down ratio for NMOS inverter driven through one or more pass transistors, alternative forms of pull up latch up in CMOS circuits

4. Basic Circuits concepts

Sheet resistance, Sheet resistance applied to MOS Transistors and inverters, Area capacitance of layers, standard unit of capacitance, delay unit, inverter delay, driving large capacitive loads, propagation delays,

5. Design Rules & Scaling:

MOS Layers, Stick diagram design rules & layout, Scaling models & scaling factors, Scaling factors device parameters, Limitations on scaling

6. Combinational Circuit Designs :

Realization of Boolean expressions, Multiplexers, Full Adders, Code Converters

7. Sequential MOS Logic Circuits:

Introduction, Behavior Bi-stable element, SR Latch, Clock Latch & Flip-Flop, CMOS , D Latch, Edged Triggered Flip-flop, Shift & rotation operation,

8. Advance CMOS Logic

Mirror Circuits, pseudo N MOS, Tri State Circuits, Clocked CMOS, Dynamic CMOS, Dual rail logic network Bi- CMOS logic

9 RF and passive IC components;

CMOS Amplifier design, BJT amplifier design, RF communication circuits, Switched capacitors, High frequency amplifier design, Operational transconductance amplifier, Multiple transistor amplifier, Small signal models of MOS transistors, Short channel effect of MOS transistors, Current mirrors, Active loads

Reference Books :

1. Basic VLSI Design (Third Edition) By Douglas.A.Pucknell , Kamaran Eshraghian
2. CMOS Digital Integrated Circuits (Third Edition) Sung MO Kang, Yousf Leblebici
3. Introduction to VLSI Circuits & Systems – John.P.Uyemura
4. Analog Circuits and Devices (Principles and Applications in Engineering, by Wai-Kai Chen
5. Analysis and Design of Analog Integrated Circuits (4th Edition) by Paul R. Gray

PAPER-2

ASIC DESIGN (ADEC12)

1. Introduction to ASICs:

Types of ASICs, Design flow, Case study, Economics of ASICs, ASIC cell library

2. CMOS logic cells:

Combinational logic cells, Sequential Logic cells, Datapath Logic cells, I/O cells, Cell compilers

3. ASIC Library Design:

Transistor as resistors, Transistor as parasitic capacitance, Logic Effort, library cell design, library architecture

4. Gate Design:

Gate array cell design, standard cell design, datapath cell design

5. Programmable ASICs:

Antifuse, Static RAM, EPROM, EEPROM technology, Practical issues

6. Programmable ASIC I/O cells:

DC output, AC output, DC input, AC input, Clock input, Power input, Xilinx I/O Block

7. Programmable ASIC Interconnect:

Actel ACT routing resources, emlore's constant,

8. Delay

RC delay in antifuse connections, antifuse parasitic capacitance

9. ASIC Construction:

Physical design, CAD tools, estimating ASIC size, Power dissipation

Reference Books:

1. Michael John Sebastin Smith, - "Application - Specific Integrated Circuits" – Pearson Education, 2003
2. Malcolm R.Haskard; Lan. C. May, "Analog VLSI Design - NMOS and CMOS" Prentice Hall, 1998.
3. Andrew Brown, - "VLSI Circuits and Systems in Silicon", McGraw Hill, 1991.
4. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, "Field Programmable Gate Arrays"- Kluwer Academic Publishers, 1992.

PAPER 3

CAD TOOLS FOR VLSI (ADEC13)

1. Scheduling Algorithms:

Introduction, A model for scheduling problems, scheduling without and with resource constraints, scheduling algorithms for extended sequencing models, scheduling pipelined circuits

2. Resource Sharing and Binding:

Introduction, sharing and binding for resource-dominated circuits, sharing and binding for general circuits, concurrent binding and scheduling

3. Data Structure and Basic Algorithms:

Basic Terminology, Graph Search Algorithms, Computational Geometry Algorithms, Basic Data structures

4. Partitioning:

Problem Formulation, Classification of Partitioning Algorithms, Group migration Algorithms, Simulated Annealing and evolution algorithm, other partitioning algorithms

5. FloorPlanning and Pin Assignment:

Problem formulation, classification, Constraint based, Integer programming based, rectangular Dualization, simulated evolution floorplanning algorithms, chip planning, Pin assignment algorithms.

6. Placement:

Problem formulation, Classification, Simulation based, Partitioning based Placement Algorithms,

7. Global Routing:

Problem formulation, Classification, Maze routing Algorithms, Line Probe Algorithms, , shortest path based Algorithms, Steiner tree based Algorithms

8. Detailed Routing:

Problem formulation, Classification single Layer routing, General river routing, Single row routing, two layer channel routing Algorithms

9. Clock and Power Routing:

Design considerations for the clocking system, delay calculation for clock trees, Problem formulation, Clock routing Algorithms, H- tree based Algorithms, MMM Algorithms, Geometric matching based Algorithms

Reference Books:

1. Synthesis and optimization of Digital Circuits--- Giovanni De Micheli, MCH, 1994
2. Algorithms for VLSI Physical Design Automation Third Edition –Naveed Sherwani
Algorithms for VLSI Design Automation -- Sabih H. Gerez
3. Genetic Algorithms for VLSI Design, Layout & Test Automation, P. Mazumder and E. M. Rudnick, Prentice Hall PTR, 1999.
4. Algorithms & Theory of Computation Handbook, , " M. J. Atallah, ed., CRC Press, 1999.

PAPER- 4 (ELECTIVE – I)

DIGITAL CIRCUIT DESIGN USING VERILOG (ADEC111)

1. Verilog – An Introduction:

A Structural Description, Simulating the binaryToESeg Driver, Creating Ports For the Module, Creating a Test bench For a Module. Behavioral Modeling of Combinational Circuits, Procedural Modeling of Clocked Sequential Circuits, Module Hierarchy

2. Logic Synthesis:

Overview of Synthesis, Combinational Logic Using Gates and Continuous Assign, Procedural Statements to Specify Combinational Logic, Inferring Sequential Elements; Latch Inferences, Flip Flop Inferences. Inferring Tri-State Devices; Describing Finite State Machines, Finite State Machine and Data path.

3. Behavioral Modeling & Concurrent Processes:

Process Model, If-Then-Else, Loops, Multi-way Branching, Functions and Tasks, Rules of Scope and Hierarchical Names, Concurrent Processes, The Wait Statement, A Concurrent Process Example, A Simple Pipelined Processor, Disabling Named Blocks, Intra-Assignment Control and Timing Events, Procedural Continuous Assignment, Sequential and Parallel Blocks

4. Module Hierarchy & Logic Level Modeling:

Module Instantiation and Port Specifications, Parameters, Arrays of Instances, Generate Blocks, Logic Level Modeling; Introduction, Logic Gates and Nets, Continuous Assignment A Mixed Behavioral/Structural Example, Logic Delay Modeling

5. Cycle-Accurate Specification:

Cycle-Accurate Behavioral Descriptions, Cycle-Accurate Specification, Mealy/Moore Machine Specifications, Introduction to Behavioral Synthesis

6. Advanced Timing:

Verilog Timing Models, Basic Model of a Simulator, Scheduling Behavioral Models, Non-Deterministic Behavior of the Simulation Algorithm, Non-Blocking Procedural Assignments

7. User-Defined Primitives:

Combinational Primitives, Sequential Primitives, Shorthand Notation, Mixed Level- and Edge-Sensitive Primitives, Switch Level Modeling
A Dynamic MOS Shift Register Example,
Switch Level Modeling

8. Designing with PLDs, CPLDs:

Read only memories, Programmable logic arrays (PLAs), Programmable array logics (PALs), Programmable logic devices (PLDs), Xilinx 3000 series FPGAs,

9. Designing FPGAs

Xilinx 4000 series FPGAs, Using a one-hot state assignment, ALTERA CPLDs, ALTERA flex 10K series CPLDs.

Reference Books:

1. Verilog Hardware Description Language by THOMAS & MOORBY, 5th Edn.
2. Verilog HDL a guide to digital design & synthesis by SAMIR PALNITHKAR, Sunsoft press, 1996,
3. Verilog HDL synthesis A practical primer by J. BHASKER, Star Galaxy press, 1997.
4. Verilog Digital System Design Zainalabedin Navabi, Mcgraw Hill publications
5. VHDL Analysis and Modeling of Digital Systems, Zainalabedin Navabi, Mcgraw Hill publications

PAPER- 4 (ELECTIVE – I)

RF MICROELECTRONIC CHIP DESIGN (ADEC112)

1. Introduction to RF and wireless technology:

Complexity, design and applications. Choice of technology.

2. Basic concepts in RF design:

Non linearity and time variance, intersymbol interference, random processes and noise. Definitions of sensitivity and dynamic range, conversion gains and distortions.

3. Analog and digital modulation

RF circuits; comparison of various techniques for power efficiency. Coherent and non-coherent detections mobile RF communications.

4. Mobile communication systems

Basics of multiple access techniques. Receiver and Tx architecture and testing heterodyne homodyne image reject direct IF and sub sampled Rxs.

5. Direct conversion and two step Transmitters

BJT & MOSFET behavior at RF frequencies modeling of the transistor and SPICE models noise performance and limitation of the devices integrated parasitic elements at high frequencies and their monolithic implementations

6. Basic blocks of RF systems

Their VLSI implementation; Low noise amplifiers design in various technologies design of mixer at giga hertz frequency range various mixers their working and implementation

7. Oscillators-I

Basic topologies VCO and definition of a phase noise noise power trade off

8. Oscillators-II

Resonator less VCO design Quadrature and single side band generator Radio frequency synthesis

9. PLLS

PLLs of various RF synthesizer architectures & frequency dividers and power amplifiers design linearization techniques design issues in integrated RF filters some discussion on available CAD tools for RF VLSI designs

Reference Books:

1. B Razavi, RF microelectronics PHI PTR 1998
2. T H Lee, Design of CMOS RF ICs, Cambridge university press 1998
3. R Jacob Baker, HW Li and D.E boce CMOS circuit design layout and simulation PHI India 1998
4. Y P Tsividis Mixed Analog & Digital VLSI devices and technology Mc Graw Hill 1996
5. Behzad Razavi, RF Microelectronics, Upper Saddle River, NJ: Prentice Hall, 1998.

PAPER- 5 (ELECTIVE – II)

PLD AND FPGA(ADE121)

1. Read only memories:

Programmable logic arrays (PLAs), Programmable array logics (PALs), Programmable logic devices (PLDs);

2. FPGAs:

Xilinx 3000 series FPGAs, Designing with FPGAs, Xilinx 4000 series FPGAs, Using a one-hot state assignment, ALTERA CPLDs, ALTERA flex 10K series CPLDs

3. Hierarchy in Design:

Controllers, Mealy and Moore Machines, Meta-stability, synchronization

4. FSM issues:

Clock Trees, Clock skew, Pipelining, Multiple clock domains, Case studies.

5. VHDL:

Behavioral, Data Flow, Structural Models, Simulation Cycles, Process, Concurrent and Sequential Statements,

6. Loops:

Delay Models, Synthesis, FSM Coding, Library, Package

7. Functions:

Procedures, Resource sharing, Test benches, Hardware-software co-simulation

8. Bus function models FPGA:

Logic Block Architecture, Routing Architecture, Programmable Interconnections

9. Design Flow:

Xilinx Virtex-II and Altera Stratix Architectures, Device Programming, Timing Closure, Debugging, Applications, Case Study. Embedded System on Programmable Chips.

Reference Books:

1. John F Wakerly, Digital Design: Principles & Practices, Prentice Hall.
2. Kevin Skahil, VHDL for Programmable Logic, Addison Wesley.
3. PLD & FPGA Data Sheets
4. Wayne Wolf, FPGA -Based Design, Prentice-Hall, 2004
5. S. Brown, Z.Vranesic Fundamentals of Digital Logic with VHDL Design .-McGraw-Hill, 2000.

PAPER- 5 (ELECTIVE – II)
LOW POWER VLSI DESIGN (ADEC122)

1. Introduction:

Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits.
Emerging Low power approaches, Physics of power dissipation in CMOS devices.

2. Device & Technology Impact on Low Power:

Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation

3. Power estimation, Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

4. Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. Low Power Design

5. Circuit level:

Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

6. Logic level:

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

7. Low power Architecture & Systems:

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

8. Low power Clock Distribution:

Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

9. Algorithm & architectural level methodologies:

Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Reference Books:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
4. Low Power Design in Deep Sub-micron Electronics by W. Nebel and J. Mermet, Kluwer Academic Publishers, 1997
5. Gary K. Yeap, Practical Low power Digital VLSI Design, Kluwer Academic Publishers, 1998.

FINAL

PAPER 6

VLSI TECHNOLOGY & SYSTEM ON CHIP (ADEC21)

1. Environment for VLSI technology:

Clean room and safety requirements wafer cleaning processes and wet chemical etching techniques.

2. Impurity incorporation:

Solid state diffusion modeling and technology; ion implantation modeling, Technology and damage annealing, characterization of impurity profiles.

3. Oxidization:

Kinetics of SiO_2 growth both for thick, thin and ultra thin films, oxidization technologies in VLSI.

4. ULSI

Characterization of oxide films, high K and low K di-electrics for ULSI

5. Lithography:

Photo lithography, E-beam lithography and newer lithography techniques for VLSI/ULSI.

6. Soc design introduction:

Methodologies and design flows for front-end and back-end designs,

7. Guidelines for Design

Tips and guidelines for front-end and back-end designs, Modern physical design techniques.

8. Integration of IPs on SOC designs:

Low-power design techniques and methodologies, VOIP (Voice over IP) and STB (Set-Top Box)

9. Design Examples:

SOC design examples, Practical IP-based design solutions

Reference Books:

1. C.Y.Chang & S M SZE(Ed), ULSi Technology, MC Graw HillInc,1996
2. S K Gandhi, VLSI Fabrication Principles, John Wiley Inc., New York 1983
3. Design: System-on-Chip Design (3rd Edition) (Paperback) by Wayne Wolf
4. From ASICs to SOCs: A Practical Approach (Hardcover) by Farzad Nekoogar ,Faranak Nekoogar
5. Bhasker, J., Verilog HDL Synthesis – A Practical Primer, Star Galaxy Publishing, Allentown PA, 1998

PAPER 7 (ELECTIVE- III)

VLSI AND DSP-DRIVEN COMPUTER SYSTEMS (ADEC231)

1. Power Management Technologies:

Introduction, Integrated Circuits Power Technology: Processing and Packaging, Diodes and Bipolar Transistors, Metal-Oxide-Semiconductor (MOS) Transistors, DMOS Transistors, CMOS Transistors, Passive Components, A Monolithic Process Example, Packaging.

2. Discrete Power Technology:

Processing and Packaging, From Wall to Board, Power MOSFET Technology Basics, Package Technologies, Ongoing Trends

3. Circuits:

Transistors, NPN, PNP, Trans-Conductance, Transistor as Transfer-Resistor, Transistor Equations, MOS versus Bipolar Transistors, Elementary Circuits, Current Mirror, Current Source, Differential Input Stage, Differential to Single Input Stage, Operational Amplifier (Opamp), Inverting and Non-Inverting Inputs, Rail to Rail Output Operation, CMOS

4. Opamp:

Opamp Symbol and Configurations, DC Open Loop Gain, AC Open Loop Gain, Voltage Reference, Positive TC of VBE, Negative TC of VBE, Build a VBE, Building a Voltage Reference, Fractional Band-Gap Voltage Reference. Voltage Regulator, Linear versus Switching, Switching Regulators, Buck Converters, Switching Regulator Power Train,

5. DC-DC Conversion Architectures:

Valley Control Architecture, Peak and Valley Control Architectures, Transient Response of Each System, Valley Control with FAN5093, Monolithic Buck Converter, A New Design Methodology for Faster Time to Market The Design Cycle, The FAN5301, The Behavioral Model, Light Load Operation, Full Load Operation, Over-Current, One Shot, Comparator, Results, Timing, Conclusion.

6. Active Clamp:

Introduction, Application, Test Results, Comments, Battery Charging Techniques: New Solutions for Notebook Battery Chargers, High Efficiency, The Smart Battery System, Data Conversion, Fast Charge, Control Algorithm of Modern Switching Regulators: Analog or Digital, Fast Switchmode Regulators and Digital Control.

7. Offline (AC-DC) Architectures:

Offline Power Architectures, Introduction, Offline Control, PFC Architecture, DC-DC Conversion Down to Low Voltage, Future Trends, Power AC Adapter: Thermal and Electrical Design, The Challenge, AC Adapter Power Dissipation, AC Adapter Case Temperature, Active and No-load Operation, Development of a Solution.

8. Power Management of Ultraportable Devices.

Power Management of Wireless Computing and Communications Devices, The Wireless Landscape, Power Management Technologies for Wireless, Cellular Telephones, Wireless Handheld, Charge, Protection and Fuel Gauging, Convergence of Cellular Telephone and Handheld, Future Architectures, Power Management in Wireless Telephones: Subsystem Design Requirements, Smart Phone Subsystems, Display Board, Keypad Board, Main Board, Battery Pack, AC Adapter,

9. Powering Feature-Rich Handsets.

Growing Complexity and Shrinking Cycle Time, Power Management Unit. Low Dropouts (LDOs), More on Power Management Units in Cell Phones, Barriers to Up-Integration, PMU Building Blocks, CPU Regulator, Low Dropout Block, The Microcontroller, The Microcontroller Die, Processing Requirements, Microcontroller-Driven Illumination System, Color Displays and Cameras Increase Demand on Power Sources and Management, Digital Still Camera, Camera Phones, Power Minimization, Untethered Operation.

Reference Books:

1. Managing Power Electronics: VLSI and DSP-Driven Computer Systems, Nazzareno Rossetti, Wiley publications
2. Vlsi Synthesis of Dsp Kernels : Algorithmic and Architectural Transformations, by Mahesh Mehendale
3. VLSI Design Methodologies for Digital Signal Processing Architectures by Magdy A. Bayoumi - Technology – Kluwer Academic Publishers
4. Vlsi Signal Processing Technology - by E.E. jr. Swartzlander, Magdy A. Bayoumi, Kluwer Academic Publishers
5. VLSI Digital Signal Processing Systems: Design and Implementation, by Keshab K. Parhi, Wiley 1999.

PAPER 7 (ELECTIVE- III)
Nanoelectronics (ADEC232)

1. Introduction:

Trends in microelectronics and nanoelectronics.

2. Theoretical Basis of Nanoelectronics:

Problem formulation and theoretical approach, Basic concepts of quantum physics. Waves and particles, Time and length scales. Quantum and classical regimes of transport, Schrödinger equation. Normalization, averages. Separation of variables. Variational method. Perturbation theory, Spin and statistics, Quantum transport. Landauer formula, Boltzmann equation; Self-consistent approach to kinetics. Drift-diffusion, hydrodynamics.

3. Electrons in Quantum Structures:

Quantum wells. (Electron spectrum in infinitely deep square potential wells, in finite square wells, in triangular wells, density of states (DOS)); Quantum wires and quantum dots (boxes). (Spectrum, DOS); Coupled quantum structures. Superlattices. (Spectrum, DOS); Excitons in quantum structures; Coulomb impurity states. Interface defects.

4. Properties of Particular Quantum Structures:

Energy spectra of some semiconductor materials; mismatch. (Matched and mismatched structures, strained and (pseudomorphic structures); Single-heterojunction devices. Selective doping. (MOS structures, single heterostructures); Basic equations and quantitative results for a single heterostructure (simple analytical estimates, numerical analysis of selectively-doped single heterostructure, control of charge transfer); Modulation-doped quantum structures (quantum wells, n-i-p structures, delta doping).

5. Abbreviated Discussion of Lattice Vibrations in Quantum Structures:

Vibrations of atomic linear chains. (Monoatomic and diatomic chains, acoustic and optical modes, density of vibrational modes); Normal coordinates. Three dimensional case. (DOS); Phonons; Lattice vibrations in quantum structures. (Acoustic and optical modes, importance of phonons in quantum structures).

6. Abbreviated Discussion of Electron Scattering in Quantum Structures:

Elastic scattering in two-dimensional electron systems; Screening of a two-dimensional electron gas; Scattering by interface roughnesses, defects and impurities; Scattering of

electrons by acoustic phonons in quantum wells and wires; Scattering of electrons by optical phonons in quantum wells and wires.

7. Parallel Transport in Quantum Structures:

Classification of transport regimes; Linear electron transport. (Boltzmann equation., diffusion, mobility); High-field transport. (Hot electrons, streaming, velocity saturation and overshoot, Gunn effect, nonequilibrium phonons, hot-electron size effect);

8. Electrons in quantum structures.

Nonlinear transport in two-dimensional electron gases, quantum wires, real-space transfer of hot electrons, nonequilibrium phonons, electron and phonon confinement, heat dissipation, mutual drag.

9. Perpendicular Transport in Quantum Structures:

Double-barrier resonant tunneling. (Coherent and sequential, time-dependent Schroedinger and its numeric solution, negative differential conductivity (NDC)); Superlattices. (Transconductance, NDC, Bloch oscillations, Wannier-Stark ladder); Ballistic injection devices. Single-electron transfer and Coulomb blockade.

Reference Books:

1. V. Mitin, V. Kochelap, M. Strosio, “*Quantum Heterostructures. Microelectronics and Optoelectronics*”, Cambridge University Press, 1999. ISBN 0-521-63635-3
2. Weisbuch, B. Vinter, “*Quantum Semiconductor Structures*”, Academic Press, 1991.
3. S.M. Sze, “*High-Speed Semiconductor Devices*”, Wiley, 1990.
4. Gerald, Bastard, “*Wave Mechanics Applied to Semiconductor Heterostructures*”, Halsted Press, 1988.
5. Ia Ipatova and V. Mitin, “*Introduction to Solid State Electronics*”. Addison-Wesley, 1996. ISBN 0-201-47962-1
